14-Bit, 25Msps 125°C ADC In LQFP

FEATURES

- **Sample Rate: 25Msps**
- **–40°C to 125°C Operation**
- **Single 3V Supply (2.8V to 3.5V)**
- **Low Power: 75mW**
- **74.5dB SNR**
- **90dB SFDR**
- No Missing Codes
- Flexible Input: $1V_{P-P}$ to $2V_{P-P}$ Range
- 575MHz Full Power Bandwidth S/H
- Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Pin Compatible Family
  LTC2246H (14-Bit), LTC2226H (12-Bit)
- 48-Pin (7mm × 7mm) LQFP Package

APPLICATIONS

- Automotive
- Industrial
- Wireless and Wired Broadband Communication

DESCRIPTION

The LTC®2246H is a 14-bit 25Msps, low power 3V A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTC2246H is perfect for demanding imaging and communications applications with AC performance that includes 74.5dB SNR and 90dB SFDR.

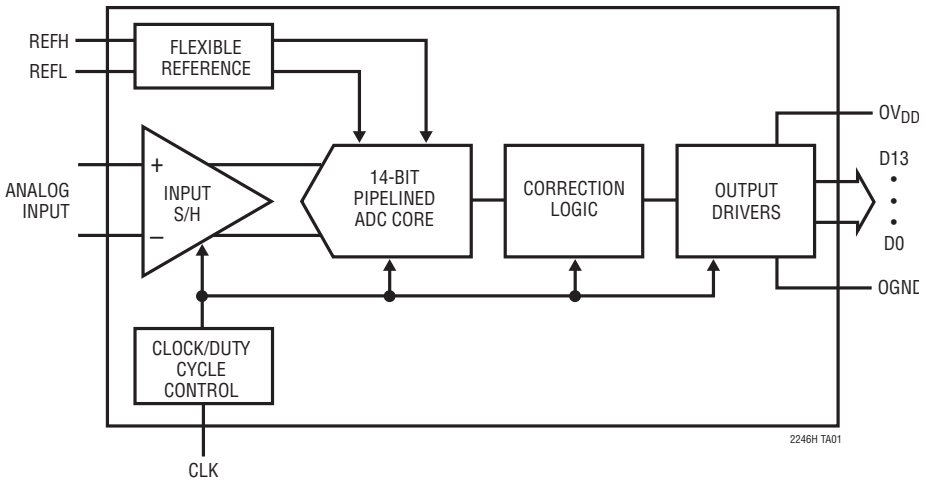
DC specs include ±1LSB INL (typ), ±0.5LSB DNL (typ) and no missing codes over temperature. The transition noise is a low $1LSB_{RMS}$.

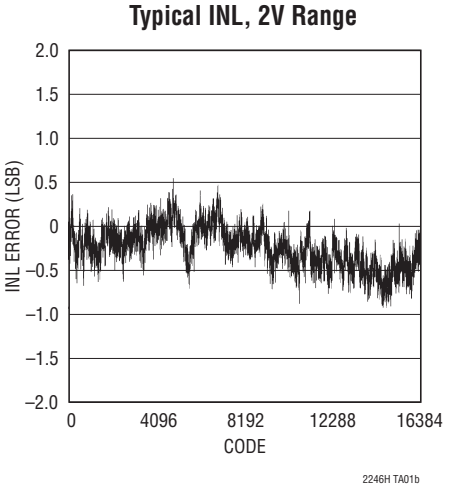
A single 3V supply allows low power operation. A separate output supply allows the outputs to drive 0.5V to 3.6V logic.

A single-ended CLK input controls converter operation. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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TYPICAL APPLICATION



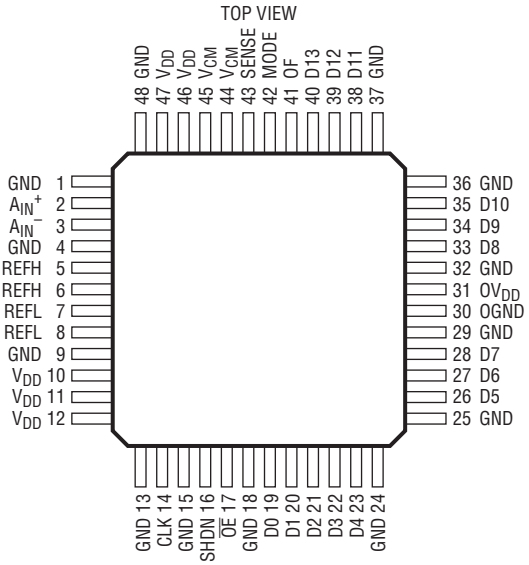


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 4V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
Analog Input Voltage (Note 3).....–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage.....–0.3V to (V_{DD} + 0.3V)
Digital Output Voltage .....–0.3V to (OV_{DD} + 0.3V)
Power Dissipation 1500mW
Operating Temperature Range..... –40°C to 125°C
Storage Temperature Range..... –65°C to 150°C

PACKAGE/ORDER INFORMATION



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP

T_{JMAX} = 150°C, θ_{JA} = 53°C/W

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2246HLX#PBF	LTC2246LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C
LEAD BASED FINISH	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2246HLX	LTC2246LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	Differential Analog Input (Note 5)	●	–6	±1	6	LSB
Differential Linearity Error	Differential Analog Input	●	–1	±0.5	1	LSB
Offset Error	(Note 6)	●	–15	±2	15	mV
Gain Error	External Reference	●	–3	±0.5	3	%FS
Offset Drift				±10		µV/°C
Full-Scale Drift	Internal Reference			±30		ppm/°C
	External Reference			±5		ppm/°C
Transition Noise	SENSE = 1V			1		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	2.8V < V_{DD} < 3.5V (Note 7)	●		±0.5V to ±1V		V
$V_{IN, CM}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Input (Note 7) Single Ended Input (Note 7)	● ●	1 0.5	1.5 1.5	1.9 2	V V
I_{IN}	Analog Input Leakage Current	0V < A_{IN}^+, A_{IN}^- < V_{DD}	●	–10		10	µA
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–10		10	µA
I_{MODE}	MODE Pin Leakage		●	–10		10	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input 12.5MHz Input 70MHz Input	 ● 	 72 	74.5 74.2 73.4	 	dB dB dB
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input 12.5MHz Input 70MHz Input	 ● 	 74 	90 90 85	 	dB dB dB
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input 12.5MHz Input 70MHz Input	 ● 	 78 	90 90 90	 	dB dB dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input 12.5MHz Input 70MHz Input	 ● 	 71.5 	74.5 74.2 73.4	 	dB dB dB
IMD	Intermodulation Distortion	f_{IN1} = 4.3MHz, f_{IN2} = 4.6MHz			90		dB

INTERNAL REFERENCE CHARACTERISTICS

T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	1.475	1.500	1.525	V
V_{CM} Output Tempco			±25		ppm/°C
V_{CM} Line Regulation	2.8V < V_{DD} < 3.5V		3		mV/V
V_{CM} Output Regulation	–1mA < I_{OUT} < 1mA		4		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS (CLK, $\overline{OE}$, SHDN)							
V_{IH}	High Level Input Voltage	V_{DD} = 3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 7)			3		pF

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
OV_{DD} = 3V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = High (Note 7)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3V			50		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –200µA	 ●	 2.7	2.995 2.99		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 1.6mA	 ●		0.005 0.09	 0.4	V V
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 9)	●	2.8	3	3.5	V
OV_{DD}	Output Supply Voltage	(Note 9)	●	0.5	3	3.6	V
I_{VDD}	Supply Current		●		25	30	mA
P_{DISS}	Power Dissipation		●		75	90	mW
P_{SHDN}	Shutdown Power	SHDN = H, $\overline{OE}$ = H, No CLK			2		mW
P_{NAP}	Nap Mode Power	SHDN = H, $\overline{OE}$ = L, No CLK			15		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 9)	●	1		25	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On (Note 7)	● ●	18.9 5	20 20	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On (Note 7)	● ●	18.9 5	20 20	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
t_D	CLK to DATA Delay	C_L = 5pF (Note 7)	●	1.4	2.7	6	ns
	Data Access Time After $\overline{OE}\downarrow$	C_L = 5pF (Note 7)	●		4.3	12	ns
	BUS Relinquish Time	(Note 7)	●		3.3	10	ns
	Pipeline Latency				5		Cycles

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3V, f_{SAMPLE} = 25MHz, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111.

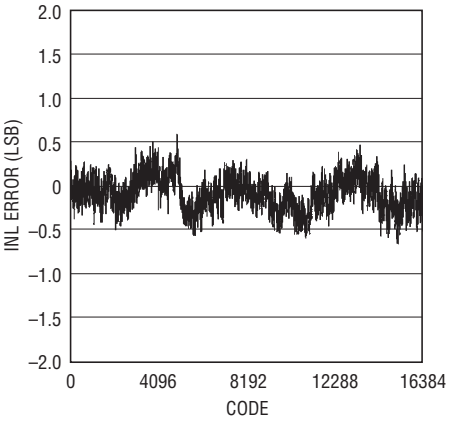
Note 7: Guaranteed by design, not subject to test.

Note 8: V_{DD} = 3V, f_{SAMPLE} = 25MHz, input range = $1V_{P-P}$ with differential drive.

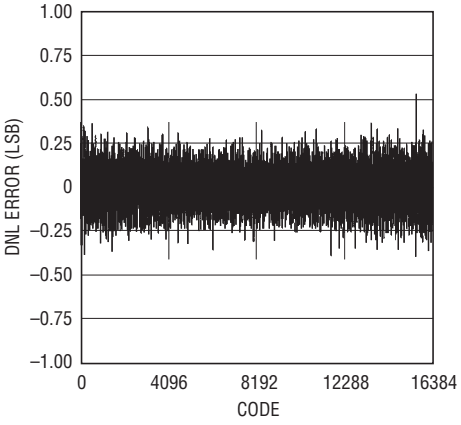
Note 9: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

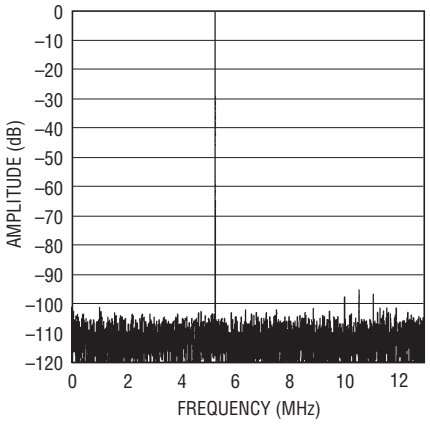
Typical INL, 2V Range, 25Msps



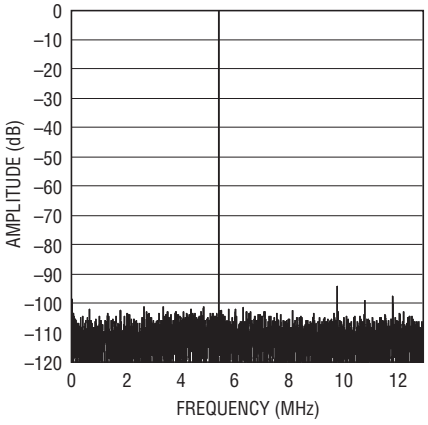
Typical DNL, 2V Range, 25Msps



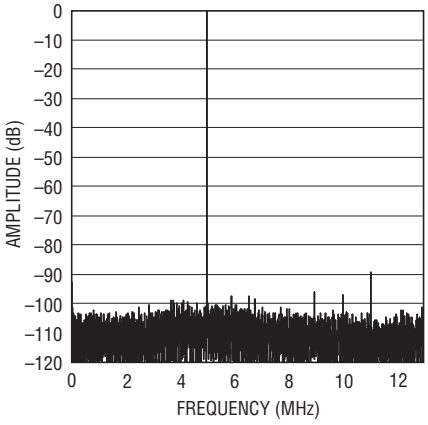
8192 Point FFT, f_{IN} = 5MHz, –1dB, 2V Range, 25Msps



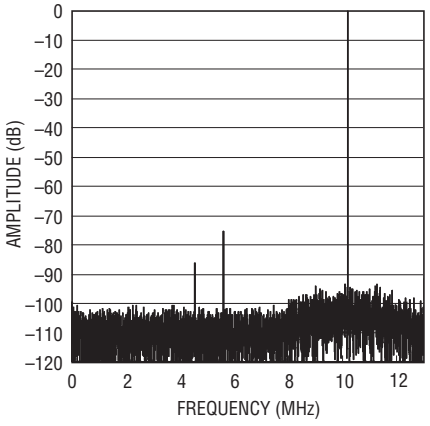
8192 Point FFT, f_{IN} = 30MHz, –1dB, 2V Range, 25Msps



8192 Point FFT, f_{IN} = 70MHz, –1dB, 2V Range, 25Msps

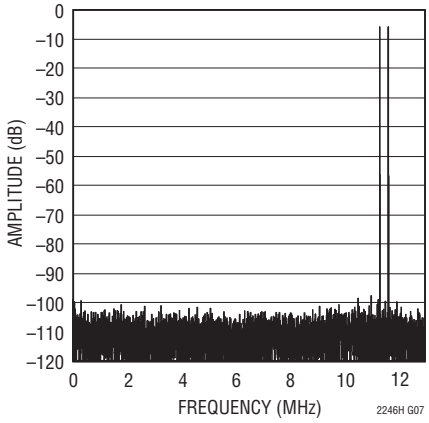


8192 Point FFT, f_{IN} = 140MHz, –1dB, 2V Range, 25Msps

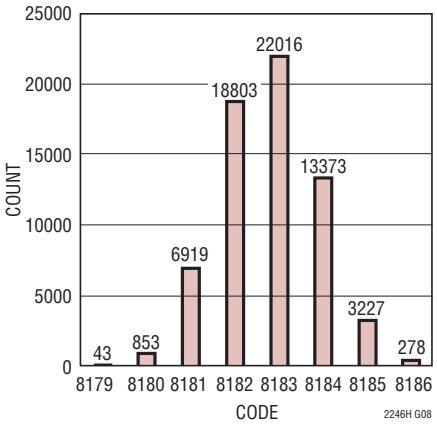


TYPICAL PERFORMANCE CHARACTERISTICS

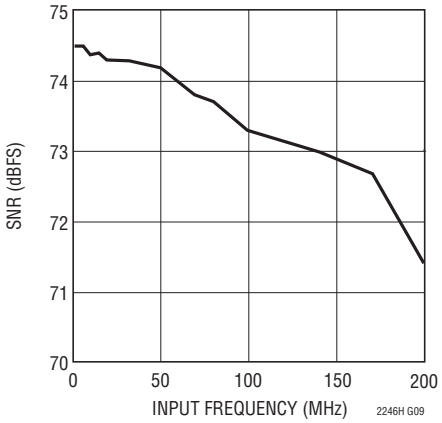
8192 Point 2-Tone FFT, f_{IN} = 10.9MHz and 13.8MHz, –1dB, 2V Range, 25Msps



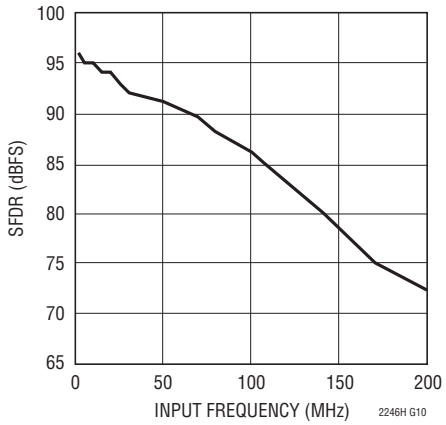
Grounded Input Histogram, 25Msps



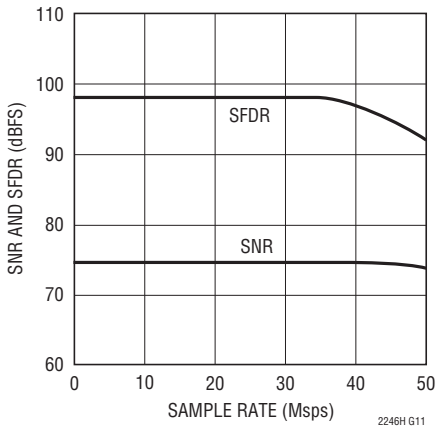
SNR vs Input Frequency, –1dB, 2V Range, 25Msps



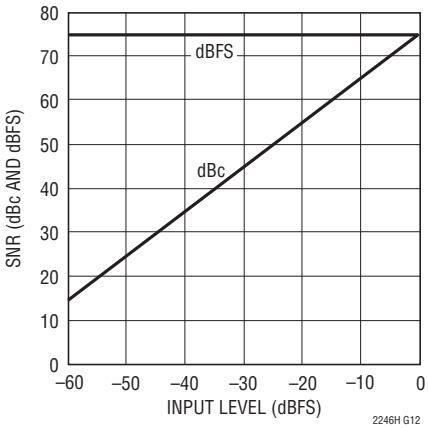
SFDR vs Input Frequency, –1dB, 2V Range, 25Msps



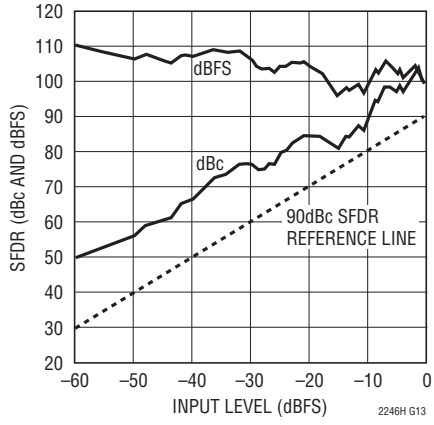
SNR and SFDR vs Sample Rate, 2V Range, f_{IN} = 5MHz, –1dB



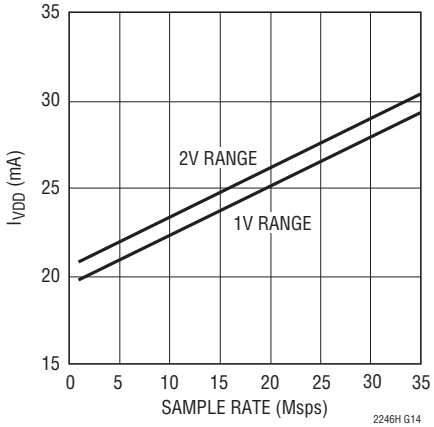
SNR vs Input Level, f_{IN} = 5MHz, 2V Range, –1dB



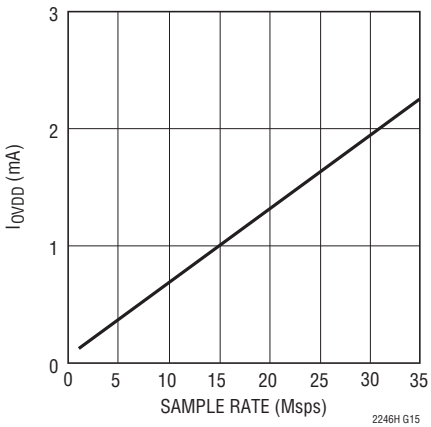
SFDR vs Input Level, f_{IN} = 5MHz, 2V Range, 25Msps



I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, O_{VDD} = 1.8V



PIN FUNCTIONS

GND (Pins 1, 4, 9, 13, 15, 18, 24, 25, 29, 32, 36, 37, 48): ADC Power Ground.

A_{IN}^+ (Pin 2): Positive Differential Analog Input.

A_{IN}^- (Pin 3): Negative Differential Analog Input.

REFH (Pins 5, 6): ADC High Reference. Bypass to Pins 7, 8 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 7, 8 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

REFL (Pins 7, 8): ADC Low Reference. Bypass to Pins 5, 6 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to Pins 5, 6 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

V_{DD} (Pins 10, 11, 12, 46, 47): 3V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

CLK (Pin 14): Clock Input. The input sample starts on the positive edge.

SHDN (Pin 16): Shutdown Mode Selection Pin. Connecting SHDN to GND and $\overline{OE}$ to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

If the clock duty cycle stabilizer is used, a >1µs high pulse should be applied to the SHDN pin once the power supplies are stable at power up.

$\overline{OE}$ (Pin 17): Output Enable Pin. Refer to SHDN pin function.

D0-D13 (Pins 19-23, 26-28, 33-35, 38-40): Digital Outputs. D13 is the MSB.

OGND (Pin 30): Output Driver Ground.

OV_{DD} (Pin 31): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

OF (Pin 41): Over/Under Flow Output. High when an over or under flow has occurred.

MODE (Pin 42): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to GND selects offset binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects offset binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 43): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

V_{CM} (Pin 44, 45): 1.5V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor.

FUNCTIONAL BLOCK DIAGRAM

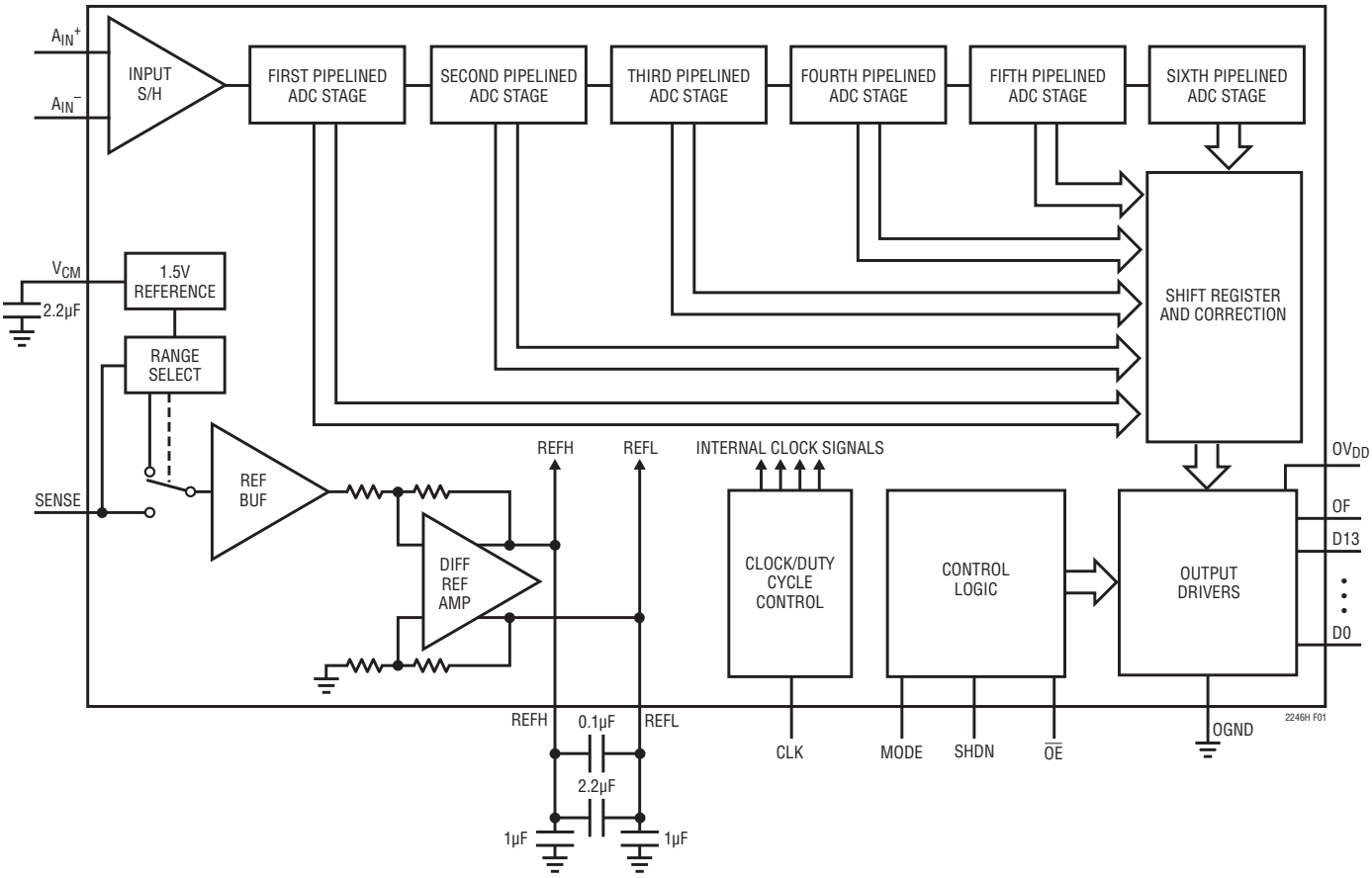
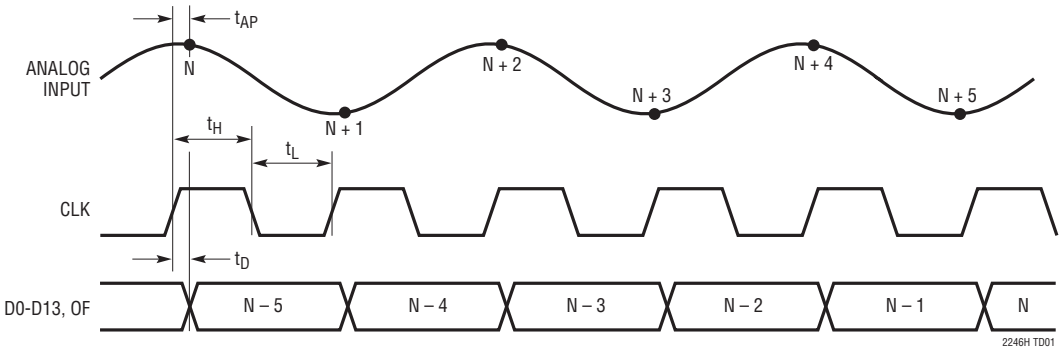


Figure 1. Functional Block Diagram

TIMING DIAGRAM



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\left(\sqrt{\left(V2^2 + V3^2 + V4^2 + ...Vn^2\right)}/V1\right)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when CLK reaches mid-supply to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log\left(2\pi \bullet f_{IN} \bullet t_{JITTER}\right)$$

CONVERTER OPERATION

As shown in Figure 1, the LTC2246H is a CMOS pipelined multistep converter. The converter has six pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost sensitive applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The CLK input is single-ended. The LTC2246H has two phases of operation, determined by the state of the CLK input pin.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the

APPLICATIONS INFORMATION

DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2246H CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when CLK is low, the transistors connect the analog inputs to the sampling capacitors and they charge to and track the differential input voltage. When CLK transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when CLK is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As CLK transitions from high to low,

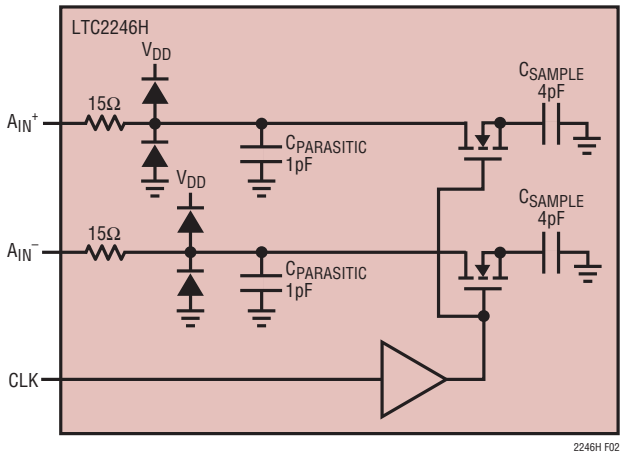


Figure 2. Equivalent Input Circuit

the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged. For a single-ended input, A_{IN}^+ should be driven with the input signal and A_{IN}^- should be connected to V_{CM} or a low noise reference voltage between 1V and 1.5V.

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing ±0.5V for the 2V range or ±0.25V for the 1V range, around a common mode voltage of 1.5V. The V_{CM} output pins (Pins 44, 45) may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pins must be bypassed to ground close to the ADC with a 2.2µF or greater capacitor.

APPLICATIONS INFORMATION

Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTC2246H can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and reactance can influence SFDR. At the falling edge of CLK, the sample-and-hold circuit will connect the 4pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when CLK rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC2246H being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Terminating on the transformer secondary is desirable, as this provides a common mode path for charging glitches caused by the sample and hold. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

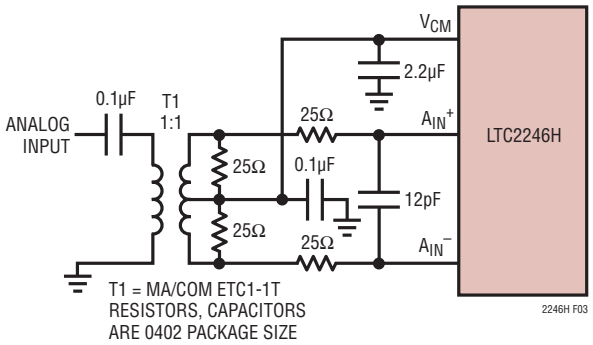


Figure 3. Single-Ended to Differential Conversion Using a Transformer

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

Figure 5 shows a single-ended input circuit. The impedance seen by the analog inputs should be matched. This circuit is not recommended if low distortion is required.

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input.

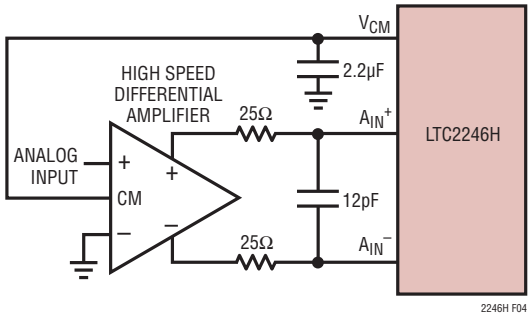


Figure 4. Differential Drive with an Amplifier

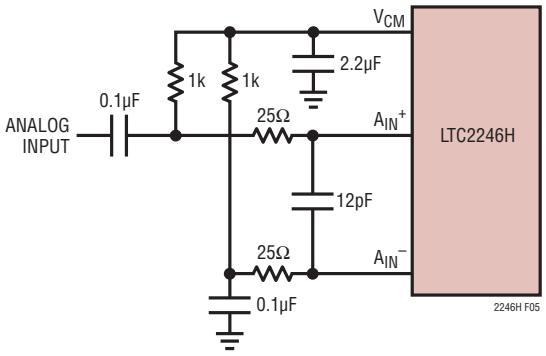


Figure 5. Single-Ended Drive

APPLICATIONS INFORMATION

Reference Operation

Figure 6 shows the LTC2246H reference circuitry consisting of a 1.5V bandgap reference, a difference amplifier and switching and control circuit. The internal voltage reference can be configured for two pin selectable input ranges of 2V (±1V differential) or 1V (±0.5V differential). Tying the SENSE pin to V_{DD} selects the 2V range; tying the SENSE pin to V_{CM} selects the 1V range.

The 1.5V bandgap reference serves two functions: its output provides a DC bias point for setting the common mode voltage of any external input circuitry; additionally, the reference is used with a difference amplifier to generate the differential reference levels needed by the internal ADC circuitry. An external bypass capacitor is required for the 1.5V reference output, V_{CM}. This provides a high frequency low impedance path to ground for internal and external circuitry.

The difference amplifier generates the high and low reference for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed.

Other voltage ranges in-between the pin selectable ranges can be programmed with two external resistors as shown in Figure 7. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor.

Input Range

The input range can be set based on the application. The 2V input range will provide the best signal-to-noise performance while maintaining excellent SFDR. The 1V input range will have better SFDR performance, but the SNR will degrade by 5.8dB.

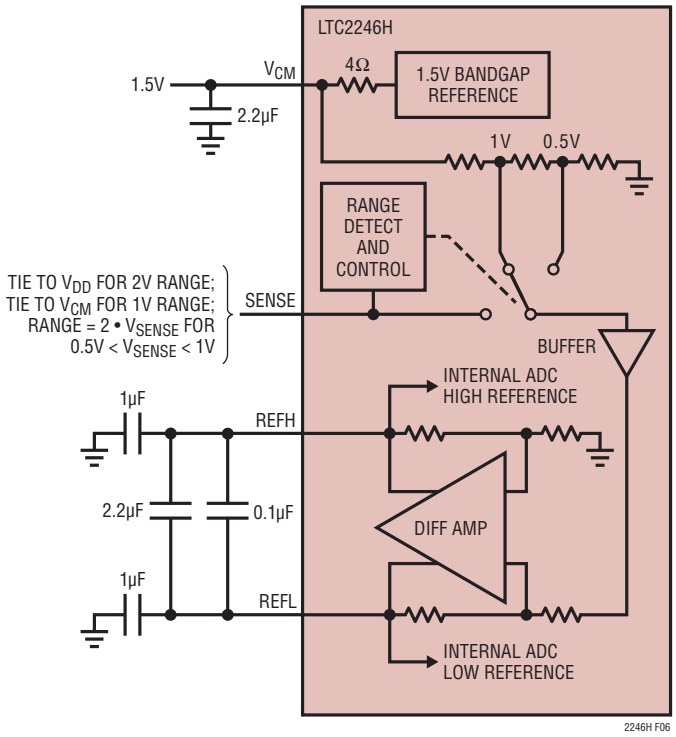


Figure 6. Equivalent Reference Circuit

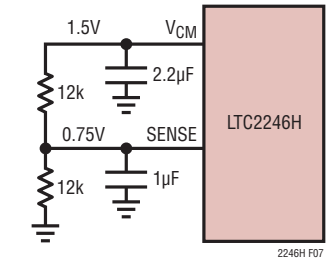
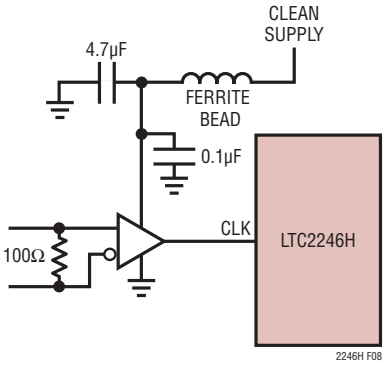


Figure 7. 1.5V Range ADC



IF LVDS USE FIN1002 OR FIN1018.
FOR PECL, USE AZ1000ELT21 OR SIMILAR

Figure 8. CLK Drive Using an LVDS or PECL to CMOS Converter

APPLICATIONS INFORMATION

Driving the Clock Input

The CLK input can be driven directly with a CMOS or TTL level signal. A differential clock can also be used along with a low-jitter CMOS converter before the CLK pin (see Figure 8).

The noise performance of the LTC2246H can depend on the clock signal quality as much as on the analog input. Any noise present on the clock signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

Maximum and Minimum Conversion Rates

The maximum conversion rate for the LTC2246H is 25Msps. For the ADC to operate properly, the CLK signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 18.9ns for the ADC internal circuitry to have enough settling time for proper operation.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

If the clock duty cycle stabilizer is used, a >1µs high pulse should be applied to the SHDN pin once the power supplies are stable at power up.

The lower limit of the LTC2246H sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2246H is 1Msps.

DIGITAL OUTPUTS

Table 1 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V Range)	OF	D13 – D0 (Offset Binary)	D13 – D0 (2's Complement)
>+1.000000V	1	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	0	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	0	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	0	10 0000 0000 0001	00 0000 0000 0001
0.000000V	0	10 0000 0000 0000	00 0000 0000 0000
–0.000122V	0	01 1111 1111 1111	11 1111 1111 1111
–0.000244V	0	01 1111 1111 1110	11 1111 1111 1110
–0.999878V	0	00 0000 0000 0001	10 0000 0000 0001
–1.000000V	0	00 0000 0000 0000	10 0000 0000 0000
<–1.000000V	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Buffers

Figure 9 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional

N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2246H should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

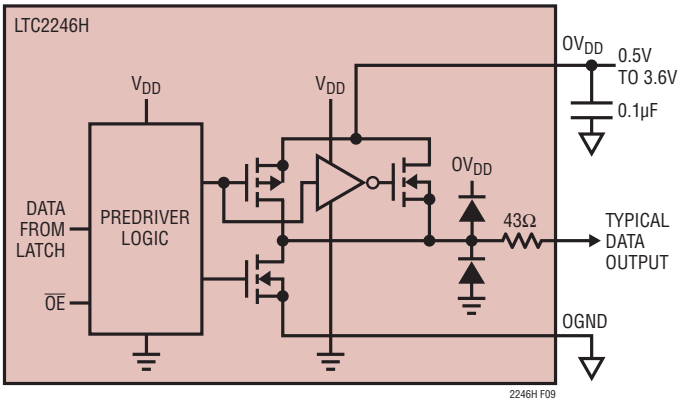


Figure 9. Digital Output Buffer

APPLICATIONS INFORMATION

Data Format

Using the MODE pin, the LTC2246H parallel digital output can be selected for offset binary or 2's complement format. Connecting MODE to GND or $1/3V_{DD}$ selects offset binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format.

An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 2 shows the logic states for the MODE pin.

Table 2. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

When OF outputs a logic high the converter is either overranged or underranged.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage from 500mV up to 3.6V. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ high disables all data outputs including OF.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode, which typically dissipates 15mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Grounding and Bypassing

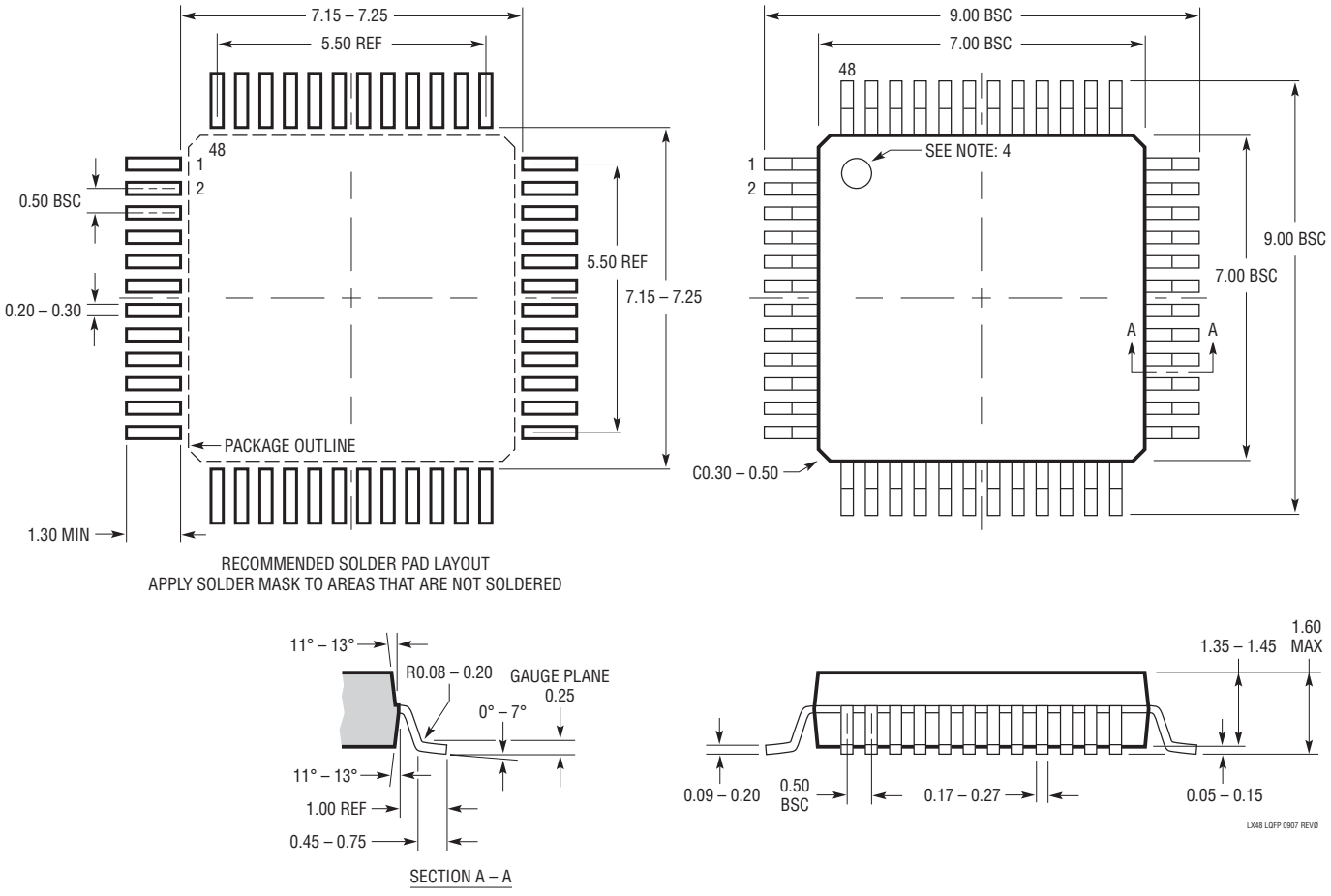
The LTC2246H requires a printed circuit board with a clean, unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, REFH, and REFL pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance is the 0.1µF capacitor between REFH and REFL. This capacitor should be placed as close to the device as possible (1.5mm or less). A size 0402 ceramic capacitor is recommended. The large 2.2µF capacitor between REFH and REFL can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2246H differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

PACKAGE DESCRIPTION

LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev Ø)



NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/11	Removed Tape and Reel information from Order Information	2

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1748	14-Bit, 80Msps, 5V ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1750	14-Bit, 80Msps, 5V Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LT1993-2	High Speed Differential Op Amp	800MHz BW, –70dBc Distortion at 70MHz, 6dB Gain
LT1994	Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	Low Distortion: –94dBc at 1MHz
LTC2202	16-Bit, 10Msps, 3.3V ADC, Lowest Noise	150mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 78dB SNR, 100dB SFDR, 64-Pin QFN
LTC2220-1	12-Bit, 185Msps, 3.3V ADC, LVDS Outputs	910mW, 67.7dB SNR, 80dB SFDR, 64-Pin QFN
LTC2224	12-Bit, 135Msps, 3.3V ADC, High IF Sampling	630mW, 67.6dB SNR, 84dB SFDR, 48-Pin QFN
LTC2225	12-Bit, 10Msps, 3V ADC, Lowest Power	60mW, 71.3dB SNR, 90dB SFDR, 32-Pin QFN
LTC2226	12-Bit, 25Msps, 3V ADC, Lowest Power	75mW, 71.4dB SNR, 90dB SFDR, 32-Pin QFN
LTC2227	12-Bit, 40Msps, 3V ADC, Lowest Power	120mW, 71.4dB SNR, 90dB SFDR, 32-Pin QFN
LTC2228	12-Bit, 65Msps, 3V ADC, Lowest Power	205mW, 71.3dB SNR, 90dB SFDR, 32-Pin QFN
LTC2229	12-Bit, 80Msps, 3V ADC, Lowest Power	211mW, 70.6dB SNR, 90dB SFDR, 32-Pin QFN
LTC2236	10-Bit, 25Msps, 3V ADC, Lowest Power	75mW, 61.8dB SNR, 85dB SFDR, 32-Pin QFN
LTC2237	10-Bit, 40Msps, 3V ADC, Lowest Power	120mW, 61.8dB SNR, 85dB SFDR, 32-Pin QFN
LTC2238	10-Bit, 65Msps, 3V ADC, Lowest Power	205mW, 61.8dB SNR, 85dB SFDR, 32-Pin QFN
LTC2239	10-Bit, 80Msps, 3V ADC, Lowest Power	211mW, 61.6dB SNR, 85dB SFDR, 32-Pin QFN
LTC2245	14-Bit, 10Msps, 3V ADC, Lowest Power	60mW, 74.4dB SNR, 90dB SFDR, 32-Pin QFN
LTC2246	14-Bit, 25Msps, 3V ADC, Lowest Power	75mW, 74.5dB SNR, 90dB SFDR, 32-Pin QFN
LTC2247	14-Bit, 40Msps, 3V ADC, Lowest Power	120mW, 74.4dB SNR, 90dB SFDR, 32-Pin QFN
LTC2248	14-Bit, 65Msps, 3V ADC, Lowest Power	205mW, 74.3dB SNR, 90dB SFDR, 32-Pin QFN
LTC2249	14-Bit, 80Msps, 3V ADC, Lowest Power	222mW, 73dB SNR, 90dB SFDR, 32-Pin QFN
LTC2250	10-Bit, 105Msps, 3V ADC, Lowest Power	320mW, 61.6dB SNR, 85dB SFDR, 32-Pin QFN
LTC2251	10-Bit, 125Msps, 3V ADC, Lowest Power	395mW, 61.6dB SNR, 85dB SFDR, 32-Pin QFN
LTC2252	12-Bit, 105Msps, 3V ADC, Lowest Power	320mW, 70.2dB SNR, 88dB SFDR, 32-Pin QFN
LTC2253	12-Bit, 125Msps, 3V ADC, Lowest Power	395mW, 70.2dB SNR, 88dB SFDR, 32-Pin QFN
LTC2254	14-Bit, 105Msps, 3V ADC, Lowest Power	320mW, 72.4dB SNR, 88dB SFDR, 32-Pin QFN
LTC2255	14-Bit, 125Msps, 3V ADC, Lowest Power	395mW, 72.5dB SNR, 88dB SFDR, 32-Pin QFN
LTC2284	14-Bit, Dual, 105Msps, 3V ADC, Low Crosstalk	540mW, 72.4dB SNR, 88dB SFDR, 64-Pin QFN
LT5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz to 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 20dBm at 1.9GHz,
LT5516	800MHz to 1.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 21.5dBm at 900MHz,
LT5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz,
LT5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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